Advanced tools and techniques for delayering and cross-sectioning semiconductor devices

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Introduction

Constantly evolving microelectronic device designs continue to grow more complex, more compact, and smaller. The designs may include an increasing number of layers, three-dimensional (3D) vertical stacking, air gaps, and different material compositions (e.g., Si₃N₄, SiO₂, Al, Cu, W, Ti, TiN, and low-k dielectrics). For this reason, top-down delayering, which is a widely used failure analysis (FA) and quality control technique, has become very challenging. The primary challenges are looking through many dissimilar nanoscale layers and attempting to investigate different layers simultaneously [1].

Conventional mechanical sample preparation is a difficult and uncontrolled process that does not allow targeting of a specific depth or layer [1, 2]. Because of the difficulties presented by mechanical sample preparation, there has been an emergence of beam-based techniques for device delayering applications. Gallium and xenon focus ion beam (FIB) techniques have been widely employed [1, 3, 4] – both tools present limitations that include a relatively small delayering area: about 20 x 20 μm for Ga FIB [1] and about 100 x 100 μm for Xe FIB [4, 5]. This size limitation makes it impossible to prepare a large slope area with the goal of exposing all the layers simultaneously.

Cross sectioning is another commonly used technique used in microelectronics industry investigations; when combined with delayering, one can gain complete knowledge about a device's faults. Cross-sectioning is often done by cleaving, mechanically polishing or, alternatively, FIB processing. As in the case of delayering, these techniques have similar limitations.

There is a need for a precise, fast, and relatively simple delayering technique for full-size wafers and for creating cross-section samples from small wafers.

This paper presents a development in semiconductor device investigation using low energy, broad-beam argon ion milling. Broad-beam argon ion milling has an advantage in that it allows material removal from larger areas [6, 7]. This technique also allows large slope area preparation, as well as a precise and controlled delayering process [7].

Experiment

The experiment was performed on two commercially available devices: 3D vertical stack memory (Samsung 3D V-NAND) and a solid-state drive (SSD) containing air gap architecture [Intel]. The devices were chosen because the elaborate structures nicely demonstrate the delayering and cross-sectioning techniques.

Cross-section sample preparation

Cross-section samples of the devices were made using the Model 1061 SEM Mill [Fischione Instruments]. The devices were cleaved and mounted on a protective mask using a cross-section loading station [Fischione Instruments], which allows positioning of the mask within 10 µm. The samples were ion milled with the following parameters: one argon ion beam, 5 kV acceleration voltage, 0° beam angle, and 20° rocking stage motion.

Delayering sample preparation

3D V-NAND flash memory top-down delayering

The 3D V-NAND flash memory top-down delayering was accomplished with the Model 1063 WaferMillTM ion beam delayering solution [Fischione Instruments], an instrument designed for pre-CD-SEM sample preparation.

The number and arrangement of the instrument's three Ar ion sources (arranged in a circle and spaced 120° apart) allow fast and uniform milling. The acceleration voltage can vary from 0.1 V to 10 kV. The beam tilt for the instrument can be adjusted from 22.5 to 32.5°. This configuration allows processing of 300 mm wafers. The delayering process was carried out at 4 keV with a 22.5° beam angle [7, 8]. The full top-down delayering duration was 50 minutes.

SSD delayering

The Model 1061 SEM Mill [Fischione Instruments] is a compact, tabletop ion mill for multiple sample preparation applications [6-12]. The instrument is fitted with two argon ion sources. The ion energy can vary from 0.1 eV to 10 keV. The beam angle can be adjusted from 0 to 10° . The chamber was designed to process $32 \times 25 \,$ mm samples. SSD delayering was done at $5 \,$ kV acceleration voltage, 3° beam angle, and 360° continuous stage rotation.

Because of the complexity of the samples' architecture and the many different materials present, the delayering process was not based on a specific material removal rate, but instead, was accomplished in two-minute steps. After each step, samples were imaged by field emission gun scanning electron microscope (FEG SEM) system and EDS data were collected.

Cross-sectioning results

Cross-section samples were prepared as a reference for the delayering samples. It is very important step in the delayering process that is done primarily to aid in determining the delayering process strategy. Cross-section samples of 3D V-NAND flash memory and SSD are shown (Figures 1 and 2) after argon ion milling at 5 keV. The EDS measurements allow the identification of all the layers that are visible in the cross-section specimens. All layers are describes in Tables 1 and 2.

Table 1: Layers identified in 3D V-NAND memory sample.

Layer shown	
in Figure 1	Layer material and purpose
a	Si ₃ N ₄ protective layer
b	SiO ₂ filling layer
С	Top TiN diffusion barrier layer
d	Al interconnection layer
e	Bottom TiN diffusion barrier layer
f	Cu bit line
g	W source line
h	W core wrapped by a Si3N4 annular
	connectors
i	Vertical W common contacts
j	3D vertical memory channel
k	3D vertical memory channel
1	3D vertical memory channel
m	3D vertical memory channel
n	3D vertical memory channel
0	3D vertical memory channel
р	3D vertical memory channel
q	3D vertical memory channel
r	Last layer (end of W common contacts)

Table 2. Layers identified IN SSD air gaps architecture

Layer shown	
in Figure 2	Layer material: thickness
a	Si ₃ N ₄ : 800 nm
b	SiO ₂ : 1000 nm
c	TiN: 50 nm
d	Al: 700 nm
e	TiN: 100 nm
f	SiO ₂ : 500 nm
g	Cu: 200 nm
h	W: 50 nm
i	Beginning of vertical W column: 450 nm
j	SiO ₂ : 250 nm
k	Si ₃ N ₄ : 80 nm
1	W: 80 nm
m	End of vertical W column: 450 nm

Delayering results: V-NAND

The first layer from the top of the 3D V-NAND flash memory is a Si_3N_4 protective layer (Figures 1a and 3a). This layer is followed by the SiO_2 fill layer (dark contrast in Figure 3). Figures 1d and 3d show the Al interconnection layer. This layer has a TiN diffusion barrier layer on the top (Figures 1c and 3c) and on the bottom (Figures 1e and 3e). In the next layer, the memory portion of the device begins. A Cu bit line (Figures 1f and 3f) connects to a W source line (Figures 1g and 3g). Round connectors can be observed (Figures 1h and 3h) beneath the W source line.

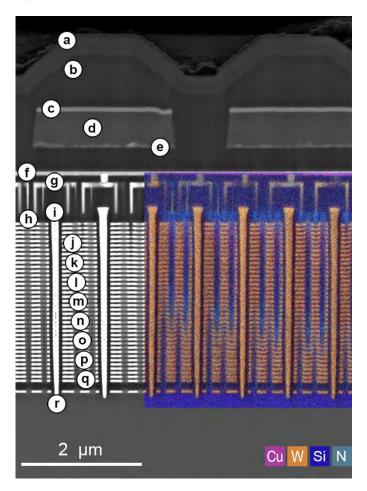
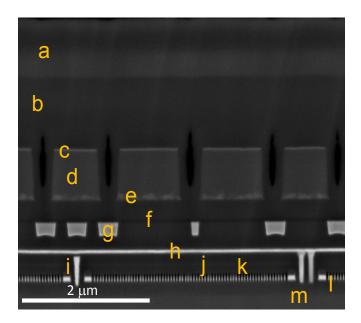


Figure 1. 3D V-NAND flash memory cross-section sample after argon ion milling at 5 keV and energy dispersive spectrometry (EDS) measurements at 3 keV. Lettered layers cross reference with layers revealed during the top-down delayering process (Figure 3).

Delayering results: SSD

The first layer from the top of the SSD air gaps device is a Si_3N_4 protective layer (Figure 2a). This layer is followed by the SiO_2 fill layer (dark contrast in Figures 2b and 4b). Figures 2d and 4d show the Al interconnection layer. This layer has a TiN diffusion barrier layer on the top (Figure 2c)

and on the bottom (Figure 2e). Figure 4f shows the Cu line and W contacts in SiO_2 , which are located at level f of the cross-section sample (Figure 2). Underneath is a Cu line (Figures 2g and 4g). A tungsten line (Figures 2h and 4h) is then observed, which is connected to vertical W columns (Figures 2i and 4i, 4m). The air gaps are formed by two parts: the top is Si_3N_4 (Figures 2k and 4k) and the bottom is W (Figures 2l and 4l).



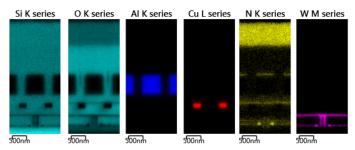


Figure 2. SSD with air gaps cross-section sample after argon ion milling at 5 keV and EDS measurements at 5 keV. Lettered layers cross reference with layers revealed during the top-down delayering process.

Conclusions

Broad-beam Ar ion milling is an accurate solution for advanced microelectronic device cross-sectioning and full top-down delayering. It reveals the 3D architecture of complex microelectronic structures layer by layer, and permits accurate targeting of specific layers for failure analyses. The results highlight that broad-beam Ar ion milling produces excellent surface quality, which allows high resolution SEM observation and EDS analyses, even at low energy.

References

- [1] DD Wang et al., AIP Adv. 5 (2015), p. 127101-127019.
- [2] AC Bonora, Solid State Technol. 20 (1977), p. 55-62.
- [3] H Yap et al., *Microelectron. Reliab.* 55 (2015), p. 1611-1616.
- [4] JV Obona et al., Microsc. Microanal. 22 (2016), p. 56-57.
- [5] R Alvis et al., Conf. Proc. Int. Symp. Test. Failure Anal. (2015) p. 1-13.
- [6] P Nowakowski et al., Microsc. Microanal. 23 (Suppl 1) (2017), p. 12-13.
- [7] P Nowakowski *et al.*, 28th Annual SEMI Advanced Semiconductor Manufacturing Conference (2017), p. 95-101.
 - URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arn umber=7969206&isnumber=7969182
- [8] P Nowakowski *et al.*, Microsc. Microanal. 23 (Suppl 1) (2017), p. 1408-1409.
- [9] P Nowakowski *et al.*, *Microsc. Microanal.* 22 (2016), p. 12–13.
- [10] P Nowakowski *et al.* European Microscopy Congress 2016: Proceedings (2016), p. 1082-1083.
- [11]P Nowakowski *et al*, European Microscopy Congress 2016: Proceedings (2016), p. 650-651.
- [12] P Nowakowski *et al.*, Microsc. Microanal. 23 (Suppl 1) (2017), p. 2224-2225.

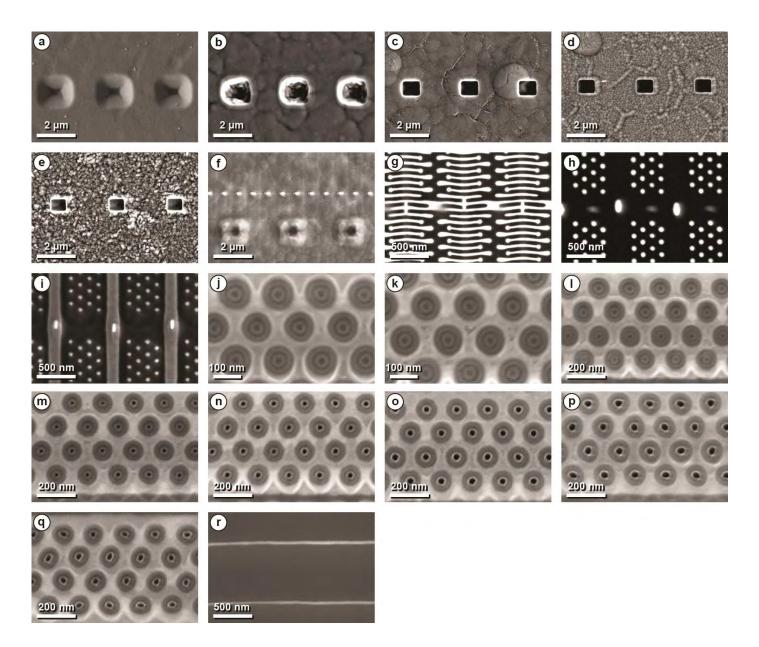


Figure 3. 3D V-NAND flash memory layers revealed by a pre-CD-SEM ion beam delayering instrument and imaged by a FEG SEM.

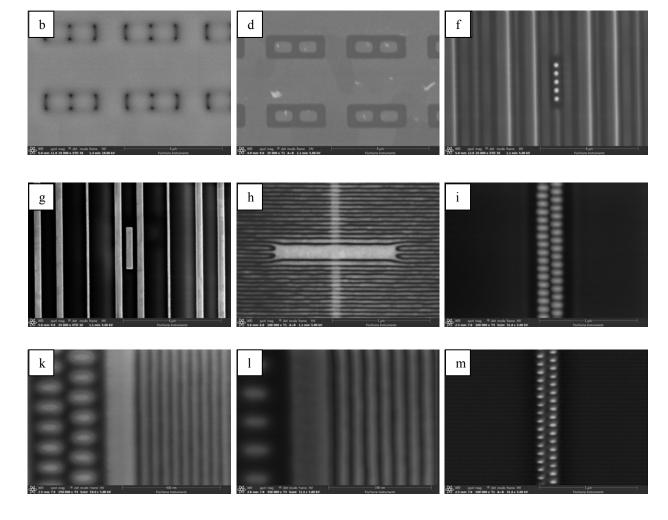


Figure 4. Air gap achitecture revealed by argon ion beam delayering process and imaged by a FEG SEM.