

Top-down delayering by low energy, broad-beam, argon ion milling – a solution for microelectronic device process control and failure analyses

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We describe a new delayering solution for semiconductor quality control and failure analyses using low-energy, broad-beam argon ion milling. The results show a large, layered area, suitable for high resolution scanning electron microscopy (SEM) investigation and energy dispersive X-ray spectroscopy (EDS) characterization. The technique allows full top-down deprocessing, layer by layer, of three-dimensional vertical NAND (3D V-NAND) flash memory devices. We show that it is possible to stop at each device layer and carry out observation and characterization. Furthermore, we demonstrate that the technique does not introduce any additional damage to the device being investigated.

Keywords – failure analysis; flash memory; ion milling; top-down deprocessing; delayering

I. INTRODUCTION

The semiconductor industry is a dynamic, rapidly growing manufacturing sector. In 2015, global sales of semiconductor products increased 9.9% and reached a record US \$335.8 billion [1]. Constantly evolving microelectronic device designs continue to grow more complex, more compact, and smaller – reaching nanoscale. For example, 3D V-NAND flash memory cells are layered vertically in three-dimensional stacks, which provides much greater cell density and increases memory capacity [2]. Such design complexity makes maintaining manufacturing quality standards a consistent challenge for the industry and failure analysis (FA) plays a critical role in meeting that challenge. Process control and FA can determine the root cause of a defective device; they enable failure identification and characterization, as well as provide feedback for product and process improvement.

Many failure analysis techniques, both nondestructive and destructive, have been developed in the past five decades [3, 4]. Nondestructive techniques include electrical measurement and testing, infrared and X-ray examination, and optical or electron microscopy evaluation. Destructive techniques include chemical etching, mechanical polishing, plasma etching, and delayering. Many techniques are untenable for multilayer devices. For example, Samsung found that etching agents are too aggressive and the company enumerated several major structural failures that can occur in NAND flash memory related to etching or particle contamination [5]. Delayering is a

popular choice because it allows top-down, whole chip characterization. The primary challenge presented by a vertical stack is looking through many dissimilar layers. FA often requires the ability to investigate different layers simultaneously [6]. A top-down delayering process that employs conventional mechanical preparation techniques has been documented as a challenging and difficult to control process that does not allow targeting of a specific depth or layer [6, 7]. Gallium- and xenon-based focused ion beam (FIB) techniques have been used for delayering of semiconductor devices [6, 8, 9]. However, in addition to causing curtaining and redisposition problems, its most important limitation is delayering of relatively small area: about 20 x 20 μm for Ga FIB [6] and about 100 x 100 μm for Xe FIB [9, 10]. That limitation makes it impossible to use a FIB system to prepare a large, sloped area that exposes all the layers simultaneously. Therefore, there is a need to develop a precise, fast, and relatively simple delayering process that overcomes these limitations.

Unlike FIB-based techniques, broad-beam argon ion milling does allow the uniform removal of large areas of material significantly greater than 100 μm , which is suitable for microelectronics layer-by-layer investigation. It enables a precise and controlled delayering process that yields a large, sloped area that allows observation of all layers simultaneously. This paper presents a new development in semiconductor device delayering for FA that uses low energy, broad-beam argon ion milling.

II. EXPERIMENT

The experiment was performed on commercially available Samsung 3D V-NAND flash memory. This device was chosen because its elaborate structure better demonstrates the delayering technique, not because of a defect investigation.

NAND (Fig. 1) is a logic gate that has two inputs, each of which can be true or false. A NAND gate produces true output only if at least one of the two operands is false, or produces false output only if all its inputs are true. Data retention in a NAND cell is based on charge trap effect, i.e., electrons are stored in silicon nitride layer [13, 14].

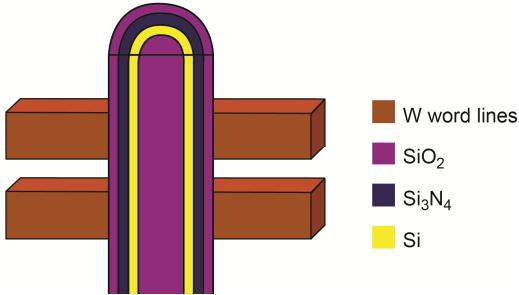


Fig. 1. Schematic illustration of 3D V-NAND memory channel. [13, 14].

A. Cross-section sample preparation

A cross-section sample of the device was made using the Model 1061 SEM Mill [Fischione Instruments] to identify all the layers. The device was cleaved and mounted on a protective mask using a cross-section loading station [Fischione Instruments], which allows positioning of the mask within 10 μm . The sample was ion milled with the following parameters: one argon ion beam, 6 keV acceleration voltage, 0° beam angle and 20° rocking stage motion. Fig. 2 shows a cross section sample of the device after ion milling.

B. Delayering sample preparation

A Model 1063 WaferMill™ ion beam delayering solution [Fischione Instruments], an instrument designed for pre-CD-SEM sample preparation, was used for 3D V-NAND flash memory top-down delayering.

The number and arrangement of the instrument's three Ar ion sources (arranged in a circle and spaced 120° apart) allow fast and uniform milling. The acceleration voltage can vary from 0.1 eV to 6 keV. The beam tilt for the instrument can be adjusted from 22.5 to 32.5°. This configuration allows processing of 300 mm wafers. The delayering process was carried out at 4 keV using 22.5° ion source tilt. The full top-down delayering duration was 50 minutes.

Because of the 3D V-NAND flash memory's complex architecture and the many different materials present, the delayering process was not based on a specific material removal rate, but instead was accomplished in two-minute steps. After each step, the 3D V-NAND flash memory was imaged by field emission gun scanning electron microscope (FEG SEM) system. A windowless detector [Oxford Instruments] that allows low voltage analyses was used to perform EDS analyses.

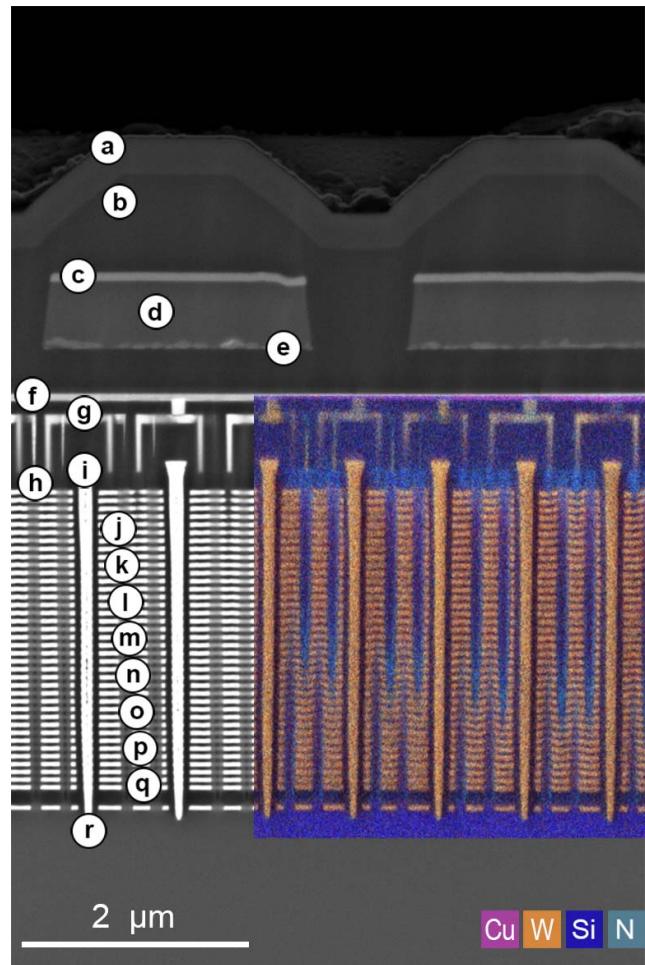


Fig. 2. 3D V-NAND flash memory cross-section sample after argon ion milling at 6 keV and energy dispersive spectrometry measurements at 3 keV. Lettered layers cross-reference with layers revealed during the top-down delayering process (Fig. 3).

III. RESULTS AND DISCUSSION

A cross-section sample was prepared as a reference for the delayering sample. Fig. 2 shows a cross-section of 3D V-NAND flash memory after argon ion milling at 6 keV. EDS mapping was carried out at 3 keV acceleration voltage on the cross-section sample, and at different stages of the delayering process. Top-down delayering images corresponding to each layer noted in the cross-section sample are shown in Fig. 3.

The second-generation, 3D V-NAND flash memory device has a total of 38 layers: 32 metal word lines, four dummy word lines, and a select gate on both the top and the bottom of the stack [5, 11, 12]. Details of the memory channels are shown in Fig. 2. The argon ion beam delayering process and EDS measurements allow the identification of all the layers that are visible in the cross-section specimen.

TABLE I. LAYERS IDENTIFIED IN BOTH THE CROSS-SECTION AND THE TOP-DOWN DELAYERING SAMPLES.

Layer shown in Figs. 2 and 3	Layer material and purpose
a	Si ₃ N ₄ protective layer
b	SiO ₂ filling layer
c	Top TiN diffusion barrier layer
d	Al interconnection layer
e	Bottom TiN diffusion barrier layer
f	Cu bit line
g	W source line
h	W core wrapped by a Si ₃ N ₄ annular connectors
i	Vertical W common contacts
j	3D vertical memory channel
k	3D vertical memory channel
l	3D vertical memory channel
m	3D vertical memory channel

n	3D vertical memory channel
o	3D vertical memory channel
p	3D vertical memory channel
q	3D vertical memory channel
r	Last layer (end of W common contacts)

The first layer from the top of the 3D V-NAND flash memory is a Si₃N₄ protective layer (Figs. 2a and 3a). This layer is followed by the SiO₂ fill layer (dark contrast in Fig. 2). Figs. 2d and 3d show the Al interconnection layer. This layer has a TiN diffusion barrier layer on the top (Figs. 2c and 3c) and on the bottom (Figs. 2e and 3e). In the next layer, the memory portion of the device begins. A Cu bit line (Figs. 2f and 3f) connects to a W source line (Figs. 2g and 3g). Round connectors can be observed (Figs. 2h and 3h) beneath the W source line. EDS measurements (Fig. 4) show that the connectors are made from a W core wrapped by a Si₃N₄ annular layer; 3D memory channels are located under the connectors.

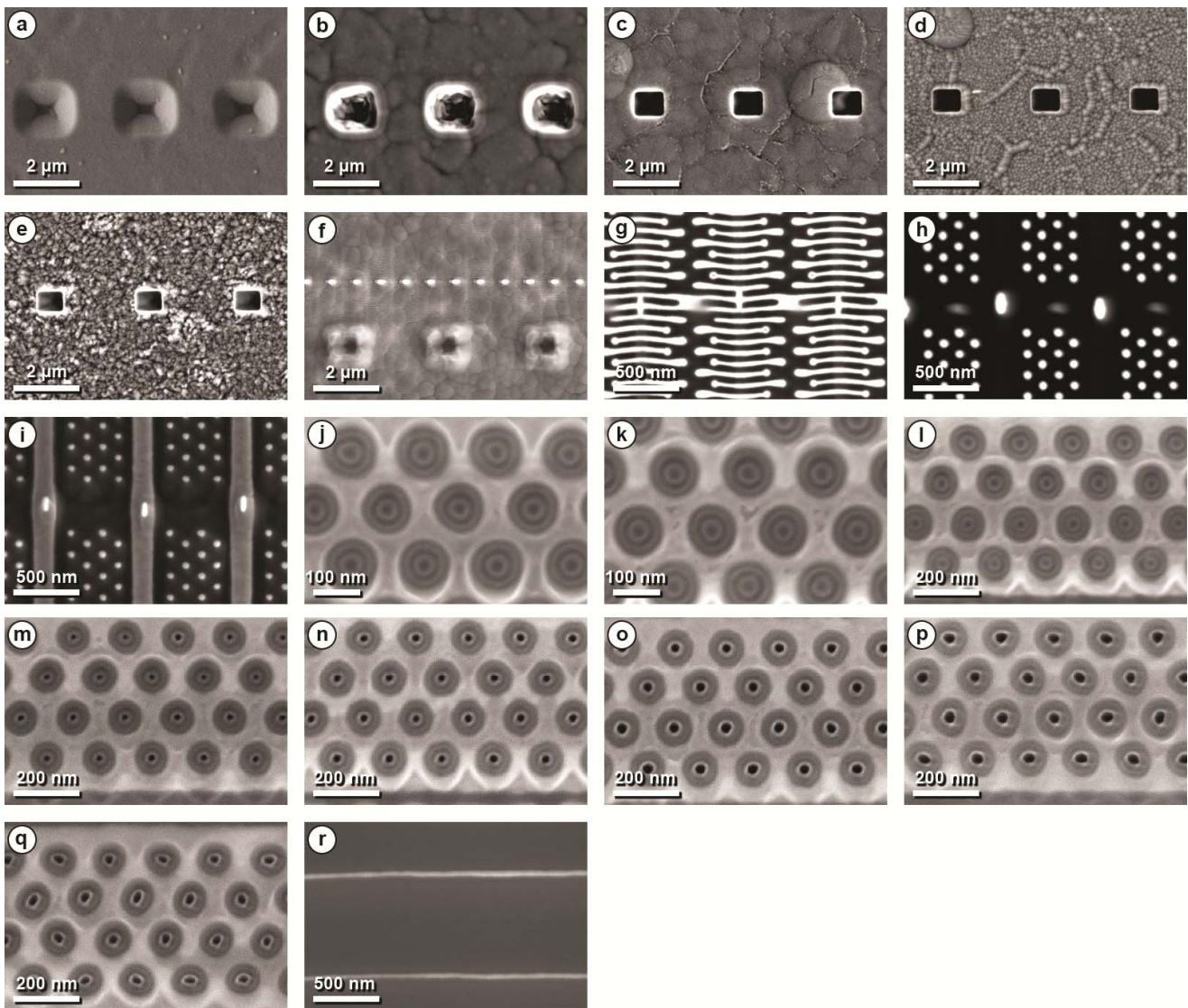


Fig. 3. 3D V-NAND flash memory layers revealed by a pre-CD-SEM ion beam delayering instrument and imaged by a FEG SEM.

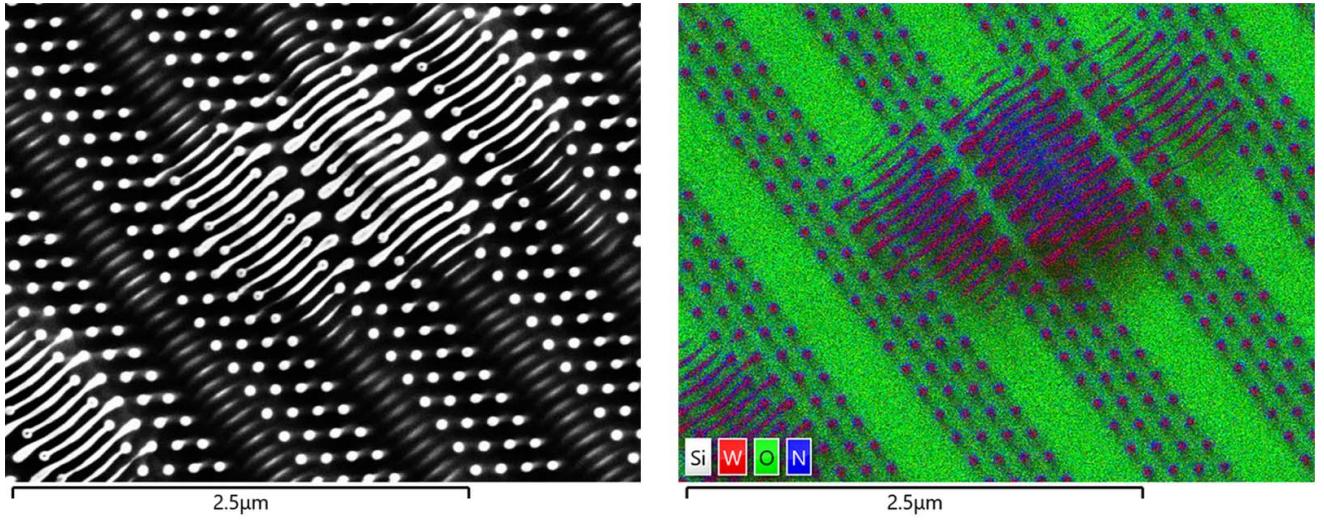


Fig. 4. SEM backscatter contrast image (left) and EDS overlay maps (right) of Si, W, O, and N show layer (h) and some of layer (g). EDS mapping was done at 3 kV SEM acceleration voltage.

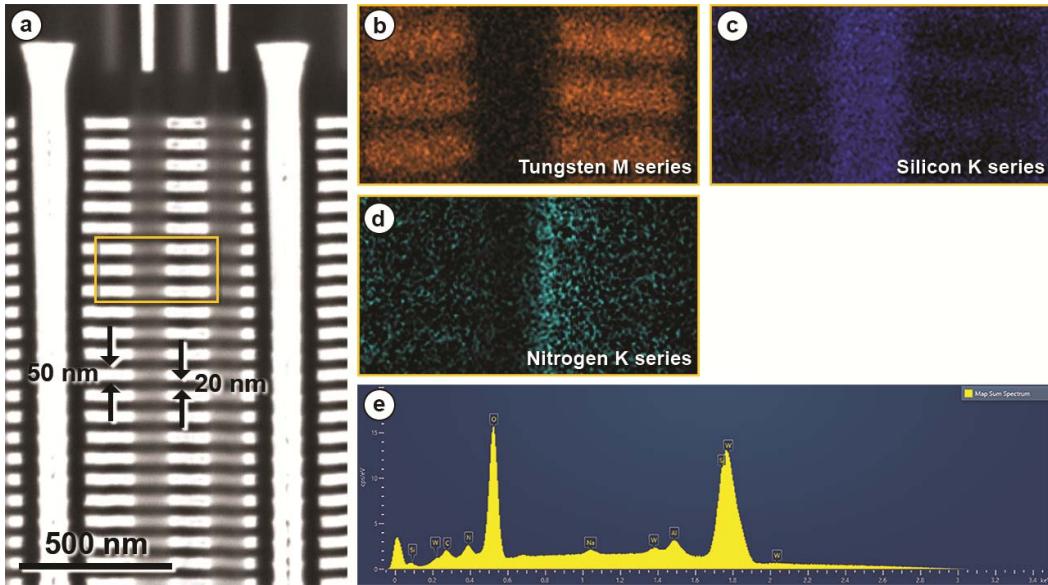


Fig. 5. SEM cross-section image of 3D V-NAND flash memory channels (a), tungsten EDS map (b), silicon EDS map (c), and nitrogen EDS map (d). The individual EDS maps correspond to the region enclosed in the yellow rectangle (a). EDS maps sum spectrum. EDS data were collected at 3 kV acceleration voltage.

On the cross-section sample image, 38 layers are observed: 32 metal word lines, 4 dummy word lines, and 2 select gates. They are separated by vertical tungsten common contacts (Figs. 2 and 3i). A vertical W contact starts above the 3D memory channels and travels through the stack to bulk silicon (Figs. 2 and 3i). On Figs. 3j – 3q, different layers (Figs. 2j – 2q) from a 3D memory stack are shown. The last layer (Fig. 2r) corresponds with Fig. 3r.

Low-energy EDS analyses carried out at 3 kV and SEM observation reveal the complex structure of 3D V-NAND vertical channel memory (Figs. 5 – 7). The 50 nm thick word lines are made from W and have 20 nm thick silicon oxide

layers in between them (Fig. 5). A very thin (~ 10 nm) Si_3N_4 layer is observed on the inner edge of the memory channel (Fig. 5d). Fig. 6 shows a plan view of the V-NAND channel corresponding to the upper layer (Fig. 2j). Each channel is 100 nm in diameter and the spacing between channels is 155 nm.

From the SEM image (Fig. 6), one can distinguish four concentric rings of thickness: 10 nm, 13 nm, 10 nm, and 13 nm (from largest to smallest diameter, respectively). However, the EDS measurements reveal five rings: Al, SiO_2 , Si_3N_4 , Si, and SiO_2 filler, respectively, from the outside to the inside of the memory channel (Fig. 7). The Si_3N_4 layer is a charge trap layer

between two silicon oxides, making a well-known oxide-nitride-oxide (ONO) structure [13, 14].

The delayering process reveals that the memory channels change and lose their round shape as the depth increases (Figs. 3j – 3q). The channels' morphology is one of the critical fabrication factors of 3D flash memory. To determine if the

elliptical shape of channels at the bottom memory levels is a physical defect or if it results from SEM beam distortion at high magnification (500,000x), electron scanning rotation from 0 to 90° was applied during observation, as shown in Fig. 8. After SEM scan rotation, the features remain distorted in the same direction. This verifies that the channels become more elliptical as one moves deeper into the device structure.

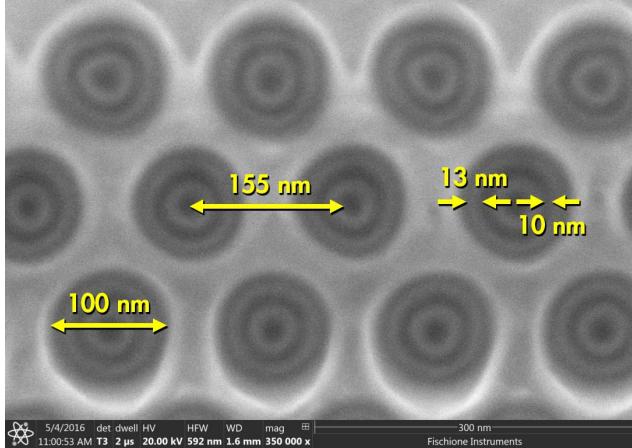


Fig. 6. SEM image showing 3D V-NAND memory channels.

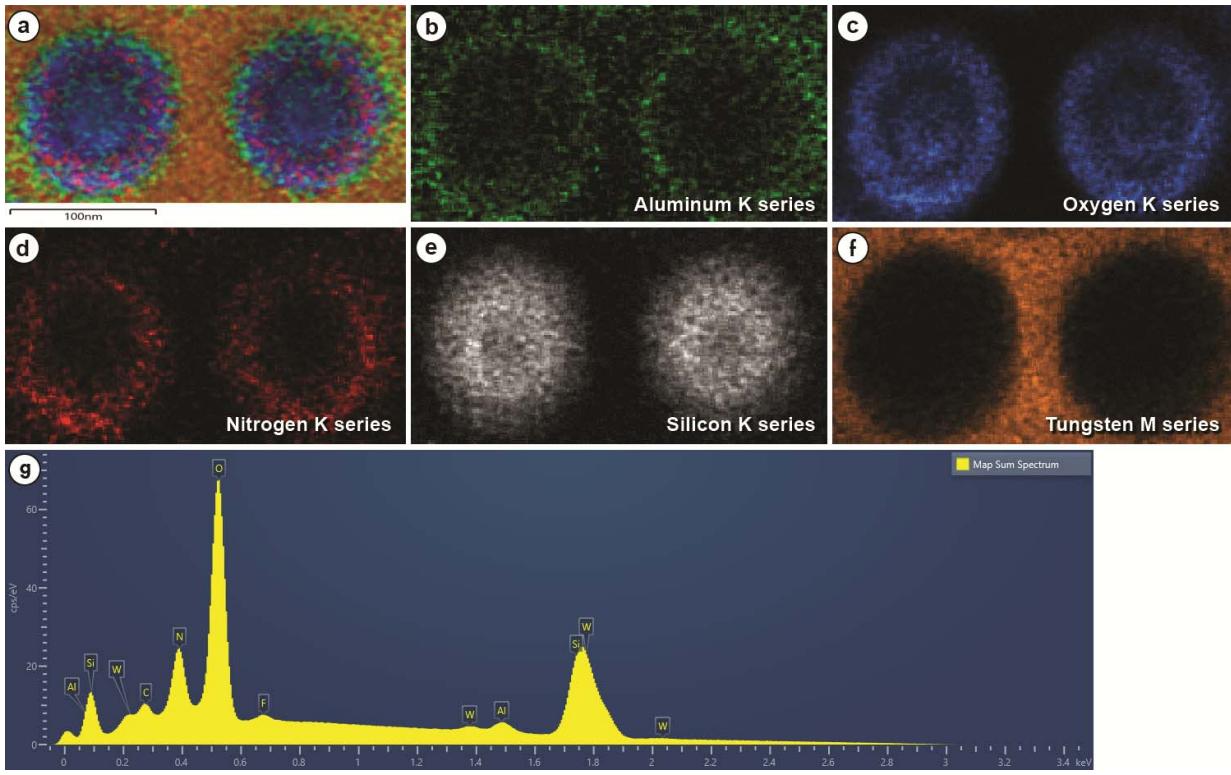


Fig. 7. EDS measurement of 3D V-NAND memory channels (show on Fig. 5) carried out at 3 keV. Overlayered EDS maps (a), aluminum K series EDS map (b), oxygen K series EDS map (c), nitrogen K series EDS map (d), silicon K series EDS map (e), tungsten M series (f), and map EDS sum spectrum (g).

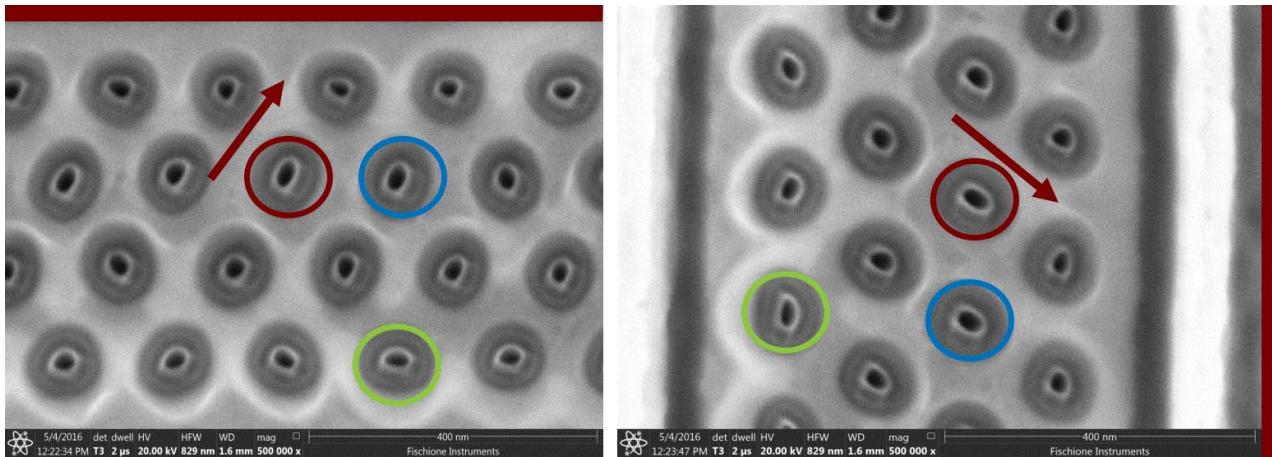


Fig. 8. 3D V-NAND memory channels morphology change as depth increases: 0° SEM scan rotation (left) and 90° SEM scan rotation (right).

IV. CONCLUSIONS

Using broad-beam Ar ion milling is an accurate solution for advanced microelectronic devices full top-down delayering. It reveals the 3D architecture of complex microelectronic structures layer by layer, permitting accurate targeting of specific layers for failure analyses. The results highlight that broad-beam Ar ion milling in a three-ion source configuration combined with rocking sample motion produces excellent surface quality, which allows high resolution SEM observation and EDS analyses, even at low energy.

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